Claims

1. A method of determining a forced gating function for at least one of a plurality of clocked state-holding elements, wherein said forced gating function compares the input and output of said at least one element, the method comprising: simulating the performance of the element for different implementation conditions; measuring the performance of the element for each condition, and determining the implementation of the forced gating function in dependence on said measured performances.

2. The method according to claim 1 wherein the step of simulating the performance of the element for different conditions further comprises simulating the performance for different types of comparison operation.

3. The method according to claim 1 wherein the different types of comparison operation comprise an XOR operation, an OR operation and a NAND operation.

4. The method according to claim 1 wherein the step of simulating the performance of the element for different conditions further comprises grouping the elements and simulating the performance for different group sizes.

5. The method according to claim 4 wherein the different group sizes include group sizes in the range of from 1 to 8.

6. The method according to claim 1 wherein the implementation of the forced gating function for each element is determined by the measured performance for all elements.

7. The method according to claim 4 further comprising the step of determining the best group size.

8. The method according to claim 7 further comprising the steps of, for each group size in turn, determining the best comparison type for each element, summing the measured performance for each group size for all elements, comparing the total

measured performance for each group size, and selecting the group size with the highest measured performance.

9. The method according to claim 8, further comprising the step of selecting the comparison type for each element.

10. The method according to claim 9 further comprising the step of selecting for each element for the selected group size, the comparison type having the highest measured performance.

11. The method according to claim 10 wherein the measured performance of each comparison type is compared to a threshold, wherein if the measured performance is below said threshold it is determined that no comparison operation is appropriate for that element.

12. The method according to claim 11 wherein each measured performance corresponds to a score, and the threshold is a zero value.

13. The method according to claim 11 wherein elements associated with a measured performance below the threshold are not associated with a gating function.

14. The method according to claim 11 wherein elements associated with a measured performance above the threshold are associated with a gating function.

15. The method according to claim 11 wherein elements having selected comparison types are grouped into groups of appropriate size.

16. The method according to claim 9 wherein a gate is created for each comparison type.

17. The method according to claim 10 wherein the gates of each group are combined.

18. The method according to claim 17 wherein combined gates comprise a gating expression for each element in the group.

19. The method according to claim 1, wherein the step of simulating the performance of the element for different conditions further comprises simulating the performance for a full-cycle clock gate and a half-cycle clock gate.

20. The method according to claim 19 further comprising selecting between a full-cycle clock gate and a half cycle clock gate, wherein the half-cycle clock gate is selected if such gate fulfills the timing requirements of a design.

21. A computer program product comprising a computer program code for determining a forced gating function for at least one of a plurality of clocked state-holding elements, wherein said forced gating function compares the input and output of said at least one element, the method comprising: simulating the performance of the element for different implementation conditions; measuring the performance of the element for each condition, and determining the implementation of the forced gating function in dependence on said measured performances.

22. An apparatus for determining a forced gating function for at least one of a plurality of clocked state-holding elements, wherein said forced gating function compares the input and output of said at least one element, the apparatus comprising: means for simulating the performance of the element for different implementation conditions; means for measuring the performance of the element for each condition; and means for determining the implementation of the forced gating function in dependence on said measured performances.

23. The apparatus according to claim 22 wherein the means for simulating the performance of the element for different conditions further comprises at least one means for simulating the performance for different types of comparison operation and means for grouping the elements and simulating the performance for different group sizes elements.

24. The apparatus according to claim 22 further comprising means for determining the forced gating function for each element in dependence on the measured performance for all elements.

25. The apparatus according to claim 22 further comprising means for simulating the performance of each element for different conditions, said simulating means further comprising means for simulating the performance for a full-cycle clock gate and a half-cycle clock gate.

26. The apparatus according to claim 25 further comprising means for selecting between a full-cycle clock gate and a half cycle clock gate, wherein a half-cycle clock gate is selected if such gate fulfills the timing requirements of a design.

27. A computer system comprising an apparatus for determining a forced gating function for at least one of a plurality of clocked state-holding elements, wherein said forced gating function compares the input and output of said at least one element, the apparatus comprising: means for simulating the performance of the element for different implementation conditions; means for measuring the performance of the element for each condition; and means for determining the implementation of the forced gating function in dependence on said measured performances.